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EXAMINER	
PLANTE, JONATHAN R	
ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/676,758	WILLIAMS ET AL.	
	Examiner	Art Unit	
	JONATHAN R. PLANTE	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08). Paper No(s)/Mail Date *03/17/2008, and 10/08/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Applicant's communication filed 05/21/2008 in response to PTO Office Action mailed 02/22/2008. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 03/17/2008 and 10/08/2008 were filed after the mailing date of the non-Final Office action on 02/22/2008. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Item CA of IDS filed 10/08/2008 was not considered for failure of Applicant to provide a copy of the cited document.

Specification Amendments

3. Acknowledgement of receiving amendments to the specification, which were received by the Office on 05/21/2008. The specification has been updated according to reflect amendments.

The objections to the Specification have been withdrawn due to amendment filed on 05/21/2008.

Drawing Amendments

4. Acknowledgement of receiving replacement drawings, which were received by the Office on 05/21/2008. These drawings are Figures 1A, 1B, 1E, 2, 4, 5A, 5D, 5E, 5F, 5G, 5H, 5I, 5J, and 6.

The objections to the drawings have been withdrawn due to amendment filed on Figures 1C, 1D, 1E, and 2.

Claim Amendments

5. Acknowledgment of receiving amendments to the claims, which were received by the Office on 05/21/2008. Claims 1-2, 15-16, 19-23, 28, and 31 are amended.

The objections to the Claims have been withdrawn due to amendment filed on 05/21/2008.

The following objections to the Claims have **NOT** been withdrawn due to amendment filed on 05/21/2008.

d. (Claim 16, Line 4): Replace "a full cache" with "the full cache" to resolve potential lack of antecedent basis issues.

g. (Claim 22, Line 3): Replace "a lower" with "the lower" to resolve potential lack of antecedent basis issues. (Amendments 05/21/2008, Line 4)

The 35 USC § 112 rejections to the Claims have been withdrawn due to amendment filed on 05/21/2008.

Response to Arguments

6. Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

7. Claims 2, 7, 12, 16, 21, and 22 are objected to because of the following informalities:

a. (Claim 2, Line 9): Replace "to host memory" with "to the host memory" to resolve potential lack of antecedent basis issues.

b. (Claim 7, Line 2): Replace "the difference" with "a difference".

c. (Claim 12, Line 2): Replace "the difference" with "a difference".

d. (Claim 16, Line 2): Replace "a full cache" with "the full cache" to resolve potential lack of antecedent basis issues.

e. (Claim 16, Line 4): Replace "a full cache" with "the full cache" to resolve potential lack of antecedent basis issues.

f. (Claim 21, Line 7): Replace "the current cache" with "a current cache" to resolve potential lack of antecedent basis issues.

g. (Claim 22, Line 4): Replace "a lower" with "the lower" to resolve potential lack of antecedent basis issues.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 20 and 22-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(Claims 1, 2, 15, 16, 20, 21, 22, and 31): Recite the limitation of "transferring a current data entry to the host system memory using a full cache line write" (Claim 1, Line 5), (Claim 2, Line 7), (Claim 16, Line 4), (Claim 20, Line 6), (Claim 21, Line 5), (Claim 22, Line 6), (Claim 31, Line 3) and also in Claim 15 recites the limitation "a partial cache line write" (Claim 15, Line 2). The usage of the term "cache line" is in conflict with the claims language in respect to system memory. The term system memory in the art commonly refers to primary memory (i.e. SRAM, DRAM, SDRAM, volatile memory, etc) and secondary memory (i.e. hard disk drives, tape drives, optical drives, and non-volatile memory) where these memories have a recognized structure and are address based in

accessing. A cache memory (i.e. 1st level cache, 2nd level cache) associated with a processor is a specialized type of memory that is structurally designed and accessed differently then system memory. As a result the Claim language is indefinite and ambiguous.

The Examiner further notes that cache line data sizes are in the range of bits 32 bits to 128 bits, while the data being transferred by descriptors are in multiple bytes, mega-bytes, gigabytes based on the amount of data to be transferred.

The Examiner will interpret the full cache line as referring to writing the full amount of data to the data queue in the system memory if there is enough available space.

(Claims 3-19, 22-32): Are rejected for incorporating the defects of the Claims from which they depend.

(Claim 20): Recites the limitation "the data queue" in Line 9. There is insufficient antecedent basis for this limitation in the claim.

The Examiner will interpret "the data queue" as meaning "the host memory" (Claim 20, Line 2).

(Claim 22): Recites the limitation "the data entries" in Line 1. There is insufficient antecedent basis for this limitation in the claim.

The Examiner will interpret "the data entries" as "data entries".

(Claims 23-32): Are rejected for incorporating the defects of the Claims from which they depend.

Appropriate correction is required.

Examiner Note: The Examiner reminds Applicant Representative of the interviews that where conducted on September 18-19, 2008 in respect to clarifying the claim language where those changes/clarification of the claim language potential can resolve the 35 USC 112 rejections above.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al. (US 6,212,593 B1 April 3, 2001), in further view of**

Arimilli et al. (US 5,491,811 February 13, 1996) and Bryg et al. (US 5,586,297 December 17, 1996).

(Claims 1, 20, and 21): Pham et al. teaches:

a. A method for transferring data entries from a peripheral to a data queue in a host memory, **[Figure 2 depicts a DMA unit using a buffer descriptor ring (Figure 4, 300) for transferring data between peripheral device (Figure 2, Index 164, 148, 146) and system memory (Figure 2, 178) where system memory contains transmit and receive buffers (Figure 3, Index 206a, 206b, 206c)]** the method comprising:

b. determining a lower limit on a number of available data entry positions in the data queue; **[The transmitting channel of the Smart DMA reads the length (equated to available data entry positions) of the corresponding buffer (equated to data queue (Figure 3, 206a-c)) by reading the BCNT (254) (byte count value) (C 1, L 42-46) where the BCNT is the size of the receive buffer (C 8, L 30)]** and

c. selectively transferring a current data entry to the data queue using a full cache line write if the lower limit is greater than or equal to a first value **[When the start of packet value (STP) value (258) and end of packet (ENP) value (260) are set the packets (equated to current data) fit into a single buffer (206) (C 7, L 64-65). Further Figure 7 depicts in Box 406 the terminal count (TC) being greater then zero data being transmitted to the buffer and when TC is equal**

to zero and the end of packet value is 1 that all data has been transferred to the buffer and the transfer is complete resulting in a full transfer of data to the data queue in the memory). Additionally the current data length can be less then the buffer byte count BCNT of the receiving buffer (C 8, L 18-20)]

Pham et al. fails to explicitly teach:

a. wherein the first value is a number related to the current cache line size, thereby preventing an overwriting of an unprocessed data entry in the data queue

Arimilli et al. teaches:

a. wherein the first value is a number related to the current cache line size, thereby preventing an overwriting of an unprocessed data entry in the data queue **["In FIG. 2, the creation, storage and use of mask bits in relation to data in I/O cache 9 is accomplished in the combination of mask bit logic block 16, mask bit register 17, read/write logic block 18, n bit wide OR gate 19, and n bit wide AND gate 21. Data transfers are in cache line wide units. Mask bit logic 16 decodes the write addresses of the data transmitted by bus aster I/O device 8 and generates byte related bits for mask bit register 17. Gate 19 determines when none of the bytes in I/O cache 9 have been modified, indicating that no action needs to be taken with references to system memory 1. Gate 21 determines when all the bytes in I/O cache 9 have been**

modified by the bus master. In the case when all n of the mask bits have been affected, the read cycle from system memory 1 is eliminated and the DMA operation is concluded with a cache line wide write from I/O cache 9 to system memory 1 upon the next cache line miss. Immediately thereafter, the mask bits are cleared. If only some of the mask bits have been modified in state, reflecting a corresponding byte written into data cache 9, processor bus controller 13 in combination with read/write logic 18 selectively enables the byte positions having unmodified bit states. Once such selective reading from system memory 1 to data cache 9 is completed, and a cache line miss occurs, the cache line in data cache 9 is transferred to system memory 1 and mask bit logic 16 is reset by processor bus controller 13 for the next successive transfer of a cache line of data from I/O device 8. The flexibility of the architecture embodied in FIG. 2 is multifaceted. First, it minimizes the read of data from system memory to I/O cache during transfers of data from an I/O bus master. This is accomplished by either completely eliminating of the read cycle, when the mask bits reflect that complete cache line has been modified, or reducing the duration of the read cycle to a minimum fraction of the cache line. Furthermore, if a purported transfer of data from the I/O device does not result in an actual writing of a cache line, the associated reading from system memory is eliminated. The use of mask bits to eliminate system memory read cycles in a reordered sequence of data transfers through a

cache has proven to be particularly valuable, in that most blocks of DMA data are significantly larger than a single cache line. Thus, the larger the block of data the greater the gain provided by the invention. The scope of the invention should be recognized to extend to transfers other than between an I/O bus master device and a system memory, such as between processor 12 and system memory 1 via processor cache 3 with the operations being refined in an analogous manner." (C 4-5, L 45-25)]

It is obvious to one skilled in the art to combine Arimilli et al. with Pham et al. using the motivation taught in Arimilli et al. of "improved rates of data transfer are obtained while providing full system memory and cache data integrity. Mask bits are created in association with blocks of data in the cache. Such masking bits allow the reordering of the transfer sequence. For data write operations in which the data completely fill the cache line, the system memory read cycle is completely eliminated. In partial cache line write situations, the extent of system memory data read is reduced to that fraction of the cache line not written."

Bryg et al. teaches:

a. wherein the first value is a number related to the current cache line size, thereby preventing an overwriting of an unprocessed data entry in the data queue **["an I/O adapter has performed DMA transfers using a data block-size that matches the size of a cache line in each system processor data cache." (C**

3, L 14-17), "In accordance with the preferred embodiment of the present invention, a method is presented which allows for a coherent write operation to be performed for a block of data which is less than a full cache line. A computing system includes a memory, an input/output adapter and a processor. The processor includes a cache. When performing a coherent write from the input/output adapter to the memory, a block of data is written from the input/output adapter to a memory location within the memory. The block of data contains less data than a full cache line in the cache. For example, a message is sent over a bus connecting the memory, the input/output adapter and the processor. The message includes an address of the memory location and a coherency index for the memory location. The cache is searched to determine whether the cache contains data for the memory location. For example, the coherency index is used in the search, if needed. When the search determines that the cache contains data for the memory location, a full cache line which contains the data for the memory location is purged. The above-described "fast" DMA method works well when DMA transactions are aligned on cache line boundaries. The DMA will eventually write the entire cache line using several coherent sub-line writes. Each coherent sub-line write will also perform a purge of the cache line in the processor caches. The second and later purges of the same cache line are usually redundant, but are needed for the case where a

processor refetches the line into its cache after the first coherent sub-line write. However, in the case where DMA transactions are not aligned on cache line boundaries, the use of "fast" DMA may result in "dirty" memory locations being purged from the cache. The I/O adapter must somehow be "informed" when it is allowed to do "fast" DMA or software must guarantee that the I/O adapter is always allowed to do "fast" DMA. In the preferred implementation, a DMA type indicator may be placed in a translation map entry along with an address of a data page in the memory. In this case, when transferring a block of data that is less than a full cache line in the cache, the value of the DMA type indicator for the data page in the memory which contains the memory location is checked. When the value of the DMA type indicates "fast" DMA may be performed, a coherent write, as described above, is performed. When the value of the DMA type indicates "fast" DMA may not be performed, a "safe" DMA transaction is performed. In a "safe" DMA transaction, a coherent read is performed to obtain the current copy of the cache line from the memory, or from a cache which contains the memory location. The cache line is modified to include the block of data. Then, the modified cache line is written back to the memory. The preferred embodiment of the present invention allows for the implementation of a fast DMA transaction for data blocks which are smaller in size than a full cache line." (C 2-3, L 52-38), "In the preferred embodiment, cache line size for cache 17 and cache 18 is thirty-two bytes.

For both fast DMA type and save DMA type, write transactions containing a full cache line of data (thirty-two bytes), and aligned on a cache line boundary, are performed as in the prior art. For both cases, I/O adapter 13 will issue a WRITE.sub.-- PURGE transaction which writes thirty-two bytes of data to a thirty-two byte aligned address in memory. The WRITE.sub.-- PURGE transaction includes a coherency index which is utilized by processor 10 and processor 11 to search for a corresponding entry in cache 17 and cache 18, respectively. If the entry is found in cache 17 or cache 18, the cache line is purged. FIG. 4 demonstrates how the second bit in page type field 33 affects performance of I/O adapter 13 on a data transaction smaller than thirty-two bytes in size (i.e., a sub-line data transaction). When I/O adapter 13 performs a sub-line write data transaction, I/O adapter 13, in a step 41 and a step 42, checks page type field 33 to determine whether the second bit of page type field 33 is cleared to logic zero, indicating fast DMA is to be performed. If fast DMA is indicated, in a step 43, a fast DMA transaction is performed. If safe DMA is indicated, in a step 44, a safe DMA transaction is performed. In order to perform a safe DMA coherent write from I/O adapter 13 to memory 12, I/O adapter 13 performs a coherent read (private) to obtain the full cache line from memory 12, cache 17 and cache 18. The full cache line is modified to include the new data. I/O adapter 13 then performs a non-coherent write

from I/O adapter 13 to memory 12 of the modified full cache line." (C 6, L 3-33)]

It is obvious to one skilled in the art to combine Bryg et al. with Pham et al. using the motivation taught in Bryg et al. of "This simplifies cache coherent DMA writes from the I/O adapter to memory. Particularly, when performing a cache coherent DMA write from an I/O adapter to memory using a data block-size that matches the size of a cache line in each system processor data cache, a coherence index may be used by each system processor to invalidate a full cache line." (C 3, L 17-23)

12. **Claims 2-19 and 22-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al., Arimilli et al., and Bryg et al. as applied to claims 1, 20, and 21 above, and further in view of Garrett et al. (US 6,334,162 B1 December 25, 2001).**

(Claims 2-3, 22): In further view of Claims 1 and 21, Pham et al. teaches:

a. The application of the data queue being a circular buffer of descriptors in the system memory (C 1, L 44-50).
b. Figure 4, depicts a 4-entry Descriptor Ring (Figure 4, 302) in the system memory (Figure 4, 178).
c. The transmit ring count (Figure 3, 202) is used to count the number of buffer descriptors with the buffer descriptor ring (Figure 3, 204).

d. Figure 8, depicts a chain of descriptors being linked together and transferred allowing for the burst transfer of descriptors.
e. A transmit buffer descriptor (Figure 5A, 208) contains status and configuration data of the buffer descriptor (C 7, L 41-44).

Pham et al. teaches the application of overflow, underflow, and other errors associated with the descriptor buffers, in addition to the linking a chain of descriptors that are processed without interruption.

However Pham et al. fails to explicitly teach the data queue being an incoming status ring.

Arimilli et al. teach:

a. a cache line write is a transfer of data to host memory **["The computer architecture in FIG. 2 depicts I/O device 8 as a bus master on I/O bus 7, and such defines that I/O bus controller 11 assumes a slave mode of operation. Thus, I/O bus controller 11 manages I/O cache 9 as a slave on I/O bus 7 in a matter analogous to the well known operation of the Micro Channel Interface Controller for the Micro Channel.TM. bus. FIG. 2 also shows processor bus controller 13 and handshake controller 14, the latter serving to coordinate the operations of bus controllers 11 and 13." (C 3, L 31-39), "In FIG. 2, the creation, storage and use of mask bits in relation to data in**

I/O cache 9 is accomplished in the combination of mask bit logic block 16, mask bit register 17, read/write logic block 18, n bit wide OR gate 19, and n bit wide AND gate 21. Data transfers are in cache line wide units. Mask bit logic 16 decodes the write addresses of the data transmitted by bus master I/O device 8 and generates byte related bits for mask bit register 17. Gate 19 determines when none of the bytes in I/O cache 9 have been modified, indicating that no action needs to be taken with references to system memory 1. Gate 21 determines when all the bytes in I/O cache 9 have been modified by the bus master. In the case when all n of the mask bits have been affected, the read cycle from system memory 1 is eliminated and the DMA operation is concluded with a cache line wide write from I/O cache 9 to system memory 1 upon the next cache line miss. Immediately thereafter, the mask bits are cleared. If only some of the mask bits have been modified in state, reflecting a corresponding byte written into data cache 9, processor bus controller 13 in combination with read/write logic 18 selectively enables the byte positions having unmodified bit states. Once such selective reading from system memory 1 to data cache 9 is completed, and a cache line miss occurs, the cache line in data cache 9 is transferred to system memory 1 and mask bit logic 16 is reset by processor bus controller 13 for the next successive transfer of a cache line of data from I/O device 8." (C 4-5, L 45-4)]

Bryg et al. teach:

a. a cache line write is a transfer of data to host memory **["In accordance with the preferred embodiment of the present invention, a method is presented which allows for a coherent write operation to be performed for a block of data which is less than a full cache line. A computing system includes a memory, an input/output adapter and a processor. The processor includes a cache. When performing a coherent write from the input/output adapter to the memory, a block of data is written from the input/output adapter to a memory location within the memory. The block of data contains less data than a full cache line in the cache. For example, a message is sent over a bus connecting the memory, the input/output adapter and the processor. The message includes an address of the memory location and a coherency index for the memory location." (C 3, L 52-65)]**

Garret et al. teaches:

a. A status queue (Figure 2, 23).

b. Burst processing of descriptors (C 3, L 65-67)

It would have been obvious to one skilled in the art to combine Pham et al. with Garret et al. to determine a lower limit on the number of available incoming data status entry positions in order to avoid the error condition of an under run situation where the

descriptor ring reads erroneous data when over running valid descriptors in the descriptor ring.

(Claim 3): In further view of Claims 2, "wherein the lower limit is determined at least in part according to a number of unused incoming data descriptors" **[The transmit ring count (Figure 3, 202) is used to count the number of buffer descriptors with the buffer descriptor ring (Figure 3, 204).].**

(Claim 4): In further view of Claims 3, Pham et al. teaches: "wherein the lower limit is determined at least in part according to a number of unused incoming data status entry positions remaining for a current incoming data descriptor" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 5): In further view of Claims 4, Pham et al. teaches: "wherein the lower limit is determined at least in part according to a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 6): In further view of Claims 5, Pham et al. teaches: "wherein determining the lower limit comprises calculating a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor minus 1." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 7): In further view of Claims 6, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line. **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 8): In further view of Claims 7, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entry positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 9): In further view of Claims 7, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 10): In further view of Claims 3, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entries positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 11): In further view of Claims 3, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 12): In further view of Claims 3, Pham et al. teaches: "wherein the number of unused incoming data descriptors is the difference between an incoming data status pointer and an incoming data descriptor write pointer." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 13): In further view of Claims 2, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entries positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 14): In further view of Claims 2, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claims 15 and 23): In further view of Claims 2 and 22, Pham et al. teaches:

a. "selectively transferring the current incoming data status entry to the host system memory using a partial cache line write if the lower limit is less than the first value" **[Depicted in Figure 6 box 406 the transfer of data continues unit the TC = 0 and ENP = 0 meaning all data has been transferred to the buffer].**

(Claim 31): In further view of Claims 2 and 22, Pham et al. teaches:

a. The application of chain descriptors together and chaining buffers together when the amount of data to be transferred exceeds the size of a buffer, the Smart DMA will use multiple buffers for the transfer of data (C 7, L 55-61).

(Claim 16): Is rejected for the same reasons as Claim 31 above since Claim 16 is broader then Claim 31.

(Claim 17): In further view of Claims 16, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entries positions remaining in the current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 18): In further view of Claims 16, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 19): In further view of Claims 16, Pham et al. teaches: "wherein determining the lower limit comprises calculating the sum of the number of Unused incoming data descriptors and the number of unused incoming data status entry positions remaining for a current incoming data descriptor minus 1" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 24): In further view of Claims 22, Pham et al. teaches: "wherein the descriptor management system determines the lower limit at least in part according to a number of unused incoming data descriptors. **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 25): In further view of Claims 24, Pham et al. teaches: "wherein the descriptor management system determines the lower limit at least in part according to a number of unused incoming data status entry positions remaining for a current incoming data descriptor. **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 26): In further view of Claims 25, Pham et al. teaches: "wherein the descriptor management system determines the lower limit at least in part according to a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 27): In further view of Claims 26, Pham et al. teaches: "wherein the descriptor management system determines the lower limit as a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor minus 1." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 28): In further view of Claims 27, Pham et al. teaches: "wherein the descriptor management system determines the number of unused incoming data descriptors as the difference between an incoming data status pointer and an incoming data descriptor write pointer." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 29): In further view of Claims 22, Pham et al. teaches: wherein the first value is a number of unused incoming data status entry positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 30): In further view of Claims 22, Pham et al. teaches: wherein the first value is a number of incoming data status entries per cache line" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 32): In further view of Claim 22, Pham et al. teaches:

a. Local Area Network Controller (C 1, L 56).

Examiner Note: The Examiner recommends that Applicant focus the amendments to the Claim language to clearly disclose in the claim language the relationship between the I/O interface, queue, and associated cache and the interdependency of those elements in respect to the atomic data transfer size being based on the cache size line.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

14. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. In addition to reference used under 35 U.S.C. 102/103, additional prior art references that disclose relevant subject matter on the merits can be found in:

a. Miller (US 5,915,104)

b. Wang (US 6,970,921)

16. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is,

indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application. **Failure to show support can result in a non-compliant response.**

When responding to this office action, Applicant is advised that if Applicant traverses an obviousness rejection under 35 U.S.C. 103, a reasoned statement must be included explaining why the Applicant believes the Office has erred substantively as to the factual findings or the conclusion of obviousness See 37 CFR 1.111(b).

Additionally Applicant is further advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday -- Thursday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. R. P./
Examiner, Art Unit 2182
December 5, 2008

/Ilwoo Park/
Primary Examiner, Art Unit 2182
December 5, 2008